REMARKS

Present Status of Application

Claims 1-11 remain pending in the application. The Office Action mailed October 20, 2004, objected the title for not being descriptive and claims 1, 3, 5-6, 8 and 10 for informalities. Claims 1-11 were rejected under U.S.C. 102(a) as being anticipated by Liu et al. (US Patent No. 6,429,536).

Claims 1, 3-6 and 8-11 have been amended. Applicant believes that these changes do not introduce new matter and reconsideration of those claims is respectfully requested. In view of the above amendments and the following discussions, a notice of allowance is respectfully solicited.

Discussion of objections

The title of the invention was objected for not being descriptive.

The title of this application has been amended as "WIRE-BONDING CHIP PACKAGE STRUCTURE AND CARRIER STRUCTURE THEREOF", to be more descriptive.

Claims 1, 3, 5-6, 8 and 10 were objected for informalities.

Claims 1, 3, 5-6, 8 and 10 have been amended to correct the informalities.

Withdrawal of these objections is respectfully requested.

Discussion for 35 U.S.C. 102 rejections

Claims 1-11 were rejected under U.S.C. 102(a) as being anticipated by Liu et al. (US Patent No. 6,429,536).

Claims 1, 4, 6, 9 and 11 have been amended to provide more detailed descriptions

according to the present invention. Supporting grounds can be found in figures 3A and 3B and the related descriptions in page 6 of the specification. As clearly shown in figure 3B, the ground contacts 214a are connected to the chip bonding area 212 (i.e. the ground contacts 214a and the chip bonding area 212 are integral). Furthermore, the ground contacts 214a are formed of a ground ring 214.

As amended for clarification purposes, independent claims 1, 4, 6, 9 and 11 respectively recite:

Claim 1. A chip package structure, comprising:

a carrier having a surface with a power contact, a ground contact and a signal contact thereon, wherein the surface also has a chip bonding area, the power contact is located close to the chip bonding area, the ground contact is connected to the chip bonding area, but the signal contact is positioned further away from the chip bonding area;

a chip having an active surface and a backside such that the backside of the chip is attached to the chip bonding area of the carrier, wherein the active surface of the chip has a plurality of bonding pads thereon;

at least a passive component having at least two electrodes positioned on the carrier such that the electrodes are bonded to said power contact and said ground contact respectively;

a plurality of first conductive wires with the two ends of each conductive wire connected to one of the bonding pads of the chip and said power contact or said ground contact;

***at least a second conductive wire with the two ends connected to one of the bonding pads of the chip and a corresponding signal contact such that the second conductive wire crosses over the passive component without contacting the passive component;** and*

an insulating material that encloses the chip, the passive component, the first conductive wires and the second conductive wire.

Claim 4. A chip carrier structure suitable for a wire-bonding package, the chip carrier structure comprising:

a carrier with a surface having a power contact, a ground contact and a signal contact thereon, wherein the surface also has a chip bonding area, the power contact is located close to the chip bonding area, the ground contact is connected to the chip bonding area, but the signal contact is positioned further away from the chip bonding area; and

at least a passive component having at least two electrodes positioned on the carrier such that the electrodes are bonded to the power contact and the ground contact respectively and the passive component is located within a region between the chip bonding area and the signal contact.

Claim 6. A chip package structure, comprising:

a carrier having a surface with a power ring, a ground ring and a plurality of signal contacts thereon, wherein the surface also has a chip bonding area, the power ring is located around the chip

bonding area, the ground ring is connected to the chip bonding area, the signal contacts are positioned further away from the chip bonding area, the power ring has a plurality of power contacts, the ground ring has a plurality of ground contacts;

a chip having an active surface and a backside such that the backside of the chip is attached to the chip bonding area of the carrier, wherein the active surface of the chip has a plurality of bonding pads thereon;

at least a passive component having at least two electrodes positioned on the carrier such that the electrodes are bonded to one of the power contacts and one of the ground contacts respectively;

a plurality of first conductive wires with the two ends of each conductive wire connected to one of the bonding pads of the chip and one of the power contacts or one of the ground contacts;

at least a second conductive wire with the two ends connected to one of the bonding pads of the chip and one of the signal contacts such that the second conductive wire crosses over the passive component without contacting the passive component; and

an insulating material that encloses the chip, the passive component, the first conductive wires and the second conductive wire.

Claim 9. A chip carrier structure suitable for a wire-bonding package, the chip carrier structure comprising:

a carrier with a surface having a power ring, a ground ring and a plurality of signal contacts thereon, wherein the surface also has a chip bonding area, the power ring is located around the chip bonding area, the ground ring is connected to the chip bonding area, the signal contacts are positioned further away from the chip bonding area, the power ring has a plurality of power contacts, the ground ring has a plurality of ground contacts; and

at least a passive component having at least two electrodes positioned on the carrier such that the electrodes are bonded to one of the power contacts and one of the ground contacts respectively.

Claim 11. A chip carrier suitable for a wire-bonding package, the chip carrier comprising a power ring, a ground ring and a plurality of signal contacts on a surface of the chip carrier, wherein the surface also has a chip bonding area, the power ring is located around the chip bonding area, the ground ring is connected to the chip bonding area, the signal contacts are positioned further away from the chip bonding area, the power ring has at least a power contact for bonding to an electrode of a passive component, the ground ring has at least a ground contact for bonding to another electrode of the passive component.

Applicant respectfully asserts that the structure of claim 1, 4, 6, 9 or 11 is patentably distinct from the prior art reference. Especially, the structure comprises "a carrier having a surface with a power contact, a ground contact and a signal contact thereon, wherein the surface also has a chip bonding area, the power contact is located close to the chip bonding area, the ground contact is connected to the chip bonding area, but the signal contact is positioned further away from the chip

bonding area" or "a carrier having a surface with a power ring, a ground ring and a plurality of signal contacts thereon, wherein the surface also has a chip bonding area, the power ring is located around the chip bonding area, the ground ring is connected to the chip bonding area, the signal contacts are positioned further away from the chip bonding area, the power ring has a plurality of power contacts, the ground ring has a plurality of ground contacts". Furthermore, the structure comprises at least "a second conductive wire with the two ends connected to one of the bonding pads of the chip and one of the signal contacts such that the second conductive wire crosses over the passive component without contacting the passive component".

Liu discloses a substrate 100 and a chip attached to a metal paddle 102, a ground ring 104, a power ring 106 on the substrate 100. As shown in Fig. 3, the ground ring 104 is separate from the metal paddle 102.

The Office Action considered Liu's metal paddle 102, ground ring 104, power ring 106 being respectively comparable to the chip bonding area, ground ring, power ring of this invention.

However, even if considering Liu's metal paddle 102 comparable to the chip bonding area of this invention, Liu's ground ring 104 is obviously different to the ground ring of this invention because the ground ring 104 is separate from the metal paddle 102.

Furthermore, Liu teaches bonding wires 140 connecting between one of the bonding pads of the chip and the power ring 106. As recognized by the Office Action, "the wires connected to the signal contacts are not shown.....", recited in page 3 of the Office Action. Even considering the bonding wires electrically connecting the bonding pads of the chip to the power ring 104, the ground ring 106 and corresponding conductive traces 108 (as recited in Liu's col. 4, lines 43-47),

Liu obviously fails to disclose the second conductive wires as recited in the present invention. Liu simply mentions possible electrical connection between the bonding pads of the chip to the conductive traces 108, but Liu does not teach or suggest such electrical connection through wires is either direct or indirect and whether the wires cross over the underlying component. Furthermore, nothing is taught or mentioned in Liu's disclosure that the wires cross over the passive component without contacting the passive component.

On the contrary, the second conductive wires of the present invention having two ends connected to one of the bonding pads of the chip and one of the signal contacts such that the second conductive wire crosses over the passive component without contacting the passive component. Consequently, spatial utilization of the carrier is increased.

Accordingly, Liu fails to teach or disclose all limitations as recited in the amended independent claim 1, 4, 6, 9 or 11. Claims depending from claims 1, 4, 6, 9 and 11 therefore are not anticipated by the reference Liu for the reasons noted above, as well as for the additional features recited therein. Therefore, reconsideration and withdrawal of these 102 rejections are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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